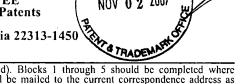
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| APPLICATION NO. FILING DATE | | | FIRST NAMED INVENTOR | | ATTORNEY DOCKET NO. CONFIRMATIO | | CONFIRMATION NO. |
| 10/757,415 | 01/15/2004 | | Hisashi Kaneko | sashi Kaneko 04173.0441 3384 | | | |
| TILE OF INVENTION: SIMULATION CIRCUIT PATTERN EVALUATION METHOD, MANUFACTURING METHOD OF SEMICONDUCTOR NTEGRATED CIRCUIT, TEST SUBSTRATE, AND TEST SUBSTRATE GROUP | | | | | | | |
| APPLN. TYPE | SMALL ENTITY | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSU | E FEE 1 | TOTAL FEE(S) DUE | DATE DUE |
| nonprovisional | NO | \$ 1400 1440 | \$300 | \$0 | | \$ 1700 - | 11/13/2007 |
| EXAMINER | | ART UNIT | CLASS-SUBCLASS | 7 | | 1740 | |
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